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EXAMINER	
HARPER, KEVIN C	

ART UNIT	PAPER NUMBER
2666	

DATE MAILED: 12/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/739,388	YOUNG, GENE F.	
	Examiner	Art Unit	
	Kevin C. Harper	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

Applicant's arguments, filed November 18, 2005, concerning claim 1 have been fully considered but they are not persuasive. Applicant argued that the Matsunami reference teaches away from Chow due to a bottleneck in JBOD access. However, in Chow each ION device must have access to the JBODs (col. 8, lines 63-67), while Matsunami similarly allows for each host device to access all disk arrays (figs. 4 and 15; col. 12, line 66 through col. 13, line 1). Although two devices must transmit through the switch, it does not appear that the packet switch of Matsunami provides excessive delay to transmitted data (figs. 5 and 7; col. 5, lines 45-55; col. 9, lines 12-24) to provide a bottleneck in the JBOD system of Chow. In Chow, there must be some delay in communication between the ION and the JBOD because of the physical nature of the system. However, Chow does not appear to disclose a limit to the delay before the system becomes inoperable. The switch of Matsunami allows any host to address to any disk as desired (col. 9, lines 12-24) and thus provides unrestricted access through the switch, as similar to the operation of the system of Chow.

Applicant's arguments, with respect to the rejection of claim 25 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Johnson.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 9-15 and 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow et al. (US 6,148,349) in view of Matsunami et al. (US 6,542,961).

1. Regarding claims 1, 6, 9-11, 15 and 18-20, Chow discloses a system module (fig. 2, item 226) to couple a switch fabric network (item 106) to shared I/O resources (items 224). The module comprises a first serverlet (figs. 2 and 3, item 212) and a second serverlet (figs. 2 and 3, item 214). The system also comprises a second switching device (fig. 8, item 802; col. 25, lines 44-50) to couple to the switch fabric network and the first and second serverlets. However, Chow does not disclose a switch and bus for coupling the serverlets to the I/O resources. Matsunami discloses processors (fig. 1, item 30) coupled to I/O resources (item 10; fig. 2) by a switch (item 20; fig. 3) and a data bus (items 31). The switch has a controller device (item 70), a switching device to couple the first interface device to the second interface device (fig. 1, item 20; note: port connections from each host to the switch), and has a third interface device (fig. 1, item 204) to couple between the second switching device and another data bus (item 21). The data bus (item 21) is coupled to the I/O resources and the controller couples the inherent second switching device to the data bus. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have a switch and bus couple serverlets to I/O resources in the invention of Chow in order to enhance scalability or improve reliability (Matsunami, col. 12, lines 4-14 and 25-40).

2. Regarding claims 2, 12 and 21, in Chow the I/O resources comprise a first disk system (fig. 2, item 218) and a second disk system (item 222).

3. Regarding claims 3-4 and 13, in Chow the serverlets each comprise memory devices and a processing unit (fig. 3, item 304), a first power conversion unit (item 306), and an inherent interface to couple the processing unit and the memory devices.

4. Regarding claims 5, 14 and 22, Chow discloses that the network (fig. 1, item 106) is Fibre Channel (col. 38, lines 7-13).

Claims 7, 16 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow et al. in view of Matsunami et al. as applied to claims 1, 11 or 20 above, and further in view of Whiting et al. (US 6,456,626).

5. Regarding claims 7, 16 and 23, Chow in view of Matsunami discloses a data bus (Matsunami, fig. 1, item 21) to couple the serverlets to the second switching device (Chow, fig. 8, item 802). However, Chow in view of Matsunami does not disclose a third switching device coupled to the switch fabric. Whiting discloses a backup network interface (fig. 5, item 150; col. 4, lines 28-32) connected to a switch fabric (item 10). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have a third switching device coupled to the switch fabric in the invention of Chow in view of Matsunami in order to provide a redundant connection to the switch fabric in the event the primary switch or interface fails.

Claims 8, 17 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow in view of Matsunami and Whiting as applied to claim 7 above, and further in view of Kaneko (US 5,739,777).

6. Regarding claims 8, 17 and 24, Chow in view of Matsunami and Whiting discloses a second switching device (fig. 8, item 802) coupled to a network (item 106). However, Chow in view of Matsunami and Whiting does not disclose a switching device comprising a first

conversion unit, a second conversion unit and a switching device to couple the switch fabric to the first and second conversion unit. Kaneko discloses a first conversion unit (fig. 1, item 8) a second conversion unit (item 9) and a switch for selecting a conversion unit. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have a first and second conversion unit and a switch in the second switching device of Chow in view of Matsunami and Whiting in order to properly format data received from a network.

Claims 25-26 and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow et al. (US 6,148,349) in view of Hipp et al. (US 6,325,636) and Johnson et al. (US 4,627,050).

7. Regarding claims 25-26 and 29, Chow discloses a system (fig. 2) comprising several serverlets (items 212 and 214) each comprising a processor and memory (fig. 3, item 304) and a power conversion unit (item 306). The serverlets are coupled to a shared disk system (fig. 2, item 218 and 222) and a switch fabric network (106). However, Chow does not disclose that the serverlets include a DIMM and that the system includes a chassis comprising first and second switching devices. Hipp discloses a system (fig. 1, item 38) comprising serverlets (item 32; fig. 2) comprising a DIMM (fig. 2, item 93; col. 10, lines 37-43), and a chassis (item 38) to house multiple serverlets. The chassis is coupled to a shared disk system (fig. 1, item 54) and includes a second switching device (fig. 1, item 40; col. 12, lines 37-40 and 47-50) to couple to a switched fabric network (item 45). The system also includes data buses (fig. 1, item 34) to connect the serverlets to the switching devices, where the first and second data buses are the same. The serverlets of the system (fig 10, item 32) do not include a cooling system (fig. 10, item 264-269). Therefore, it would have been obvious to one skilled in the art at the time the invention was

made to have a server chassis for serverlets of the invention of Chow in order to simplify or make easier the implementation of several computing resources.

8. Further, Chow in view of Hipp does not disclose a first switch coupled to a data bus. Johnson discloses a switch (fig. 2, item 11; fig. 5, note: the expander uses time slot switching - col. 10, lines 1-10 and 25-35) connected to a data bus (item 10). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have a switch coupled to a data bus in the invention of Chow in view of Hipp in order to provide increase throughput for connected modules (Johnson, col. 1, lines 21-25 and 35-44).

9. Regarding claim 30, Chow in view of Hipp and Johnson discloses serverlets that include an internal disk system (fig. 2, item 86). In removing a disk system, the scope of the serverlet is merely broadened by eliminating elements and their functions. It has been held that omission of an element and its function is an obvious expedient if the remaining elements perform the same function as before. In re Karlson, 136 USPQ 184 (CCPA). Also note Ex parte Rainu, 168 USPQ 365 (Bd. App. 1969) (omission of a reference element whose function is not needed would be obvious to one skilled in the art). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to not have an internal disk system in the invention of Chow in view of Hipp and Johnson.

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chow in view of Hipp and Johnson as applied to claim 26 above, and further in view of Aguilar et al. (US 6,199,137).

10. Chow in view of Hipp and Johnson discloses a data bus connecting switching devices. However, Chow in view of Hipp and Johnson does not disclose the data bus is Hublink. Aguilar

discloses a system bus that is Hublink, among several other standardized buses (col. 5, lines 46-48). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have a Hublink bus in the invention of Chow in view of Hipp and Johnson in order to provide fast, standardized interconnectivity between computer components.

Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chow in view of Hipp and Johnson as applied to claim 26 above, and further in view of Bealkowski et al. (US 5,465,357).

11. Chow in view of Hipp and Johnson does not disclose accessing boot information from a disk system. Bealkowski discloses accessing boot information from a disk system (fig. 1B, col. 11, lines 29-32). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to perform network booting for serverlets in the invention of Chow in view of Hipp and Johnson in order to easily provide access to an update-to-date operating system or to reduce the complexity of the serverlets.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Harper whose telephone number is 571-272-3166. The examiner can normally be reached weekdays from 11:00 AM to 7:00 PM ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema S. Rao, can be reached at 571-272-3174. The centralized fax number for the Patent Office is 571-273-8300. For non-official communications, the examiner's personal fax number is 571-273-3166 and the examiner's e-mail address is kevin.harper@uspto.gov.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications associated with a customer number is available through Private PAIR only. For more information about the PAIR system, see portal.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin C. Harper

December 5, 2005